PRACTICAL M-ARY DEMODULATOR AND METHOD OF OPERATION FOR USE IN A CDMA WIRELESS NETWORK BASE STATION

ABSTRACT OF THE DISCLOSURE

A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of the orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$. The demodulator comprises: 1) a Logic 00 input detector for comparing sequential pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic 00 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; 2) a summation circuit comprising S accumulators; 3) a Logic 00 switch array comprising S switches, wherein a Kth one of the S switches in the Logic 00 switch array couples an output of the Logic 00 input detector to a first input of a Kth one of the S accumulators; 4) a storage array for storing S code masks associated with the S orthogonal modulation codes, wherein each of the S code masks comprises M/2 code mask bits and each of the M/2 code mask bits is associated with a corresponding sequential pair of the M binary bits in one of the orthogonal modulation codes; and 5) control circuitry for synchronously applying the M/2 code mask bits in a Kth one of the S code masks in

the storage array as a switch control signal to the Kth switch in the Logic 00 switch array such that a Logic 1 code mask bit in the Kth code mask closes the Kth switch in the Logic 00 switch array whenever the Logic 00 input detector is comparing a sequential pair of the M binary bits equal to 00, thereby connecting the [+1,+1] output signals of the Logic 00 input detector to the first input of the Kth accumulator.